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10/054,247	01/22/2002	Mitchell A. Buznitsky	BP2053	3716

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EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,247	BUZNITSKY ET AL.	
	Examiner	Art Unit	
	Lana N Le	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-30,41-45 and 51-55* is/are allowed.

6)☒ Claim(s) *1,5,9,31-33,35,36 and 46-49* is/are rejected.

7)☐ Claim(s) *2-4,6-8,10,34,37-40 and 50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 31 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- claim 1, lines 10, 13, and 15, the word "substantially" is vague and indefinite since it is not clear what the received clock signal is comprised of or fails to comprise of.

- claim 31, lines 4, 7, 12, and 16, the word "substantially" is vague and indefinite since it is not clear what the received clock signal is comprised of and what the additional new clock signal is comprised of.

- claim 41, lines 5, 9, 13, and 16, 21, and 26, the word "substantially" is vague and indefinite since it is not clear what the received clock signal is comprised of and what the additional new clock signal is comprised of.

- claim 41, line 4-5, the "generating a clock signal using a low power oscillator when the operational mode comprises a low power **bypass** mode" is not clear why the low power oscillator would be used if it's low power bypass mode.

Claim Objections

3. Claim 41 is objected to because of the following informalities:

- in claim 41, line 8, "operational" should be ""operational mode".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 5, 9, and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Kohlschmidt (US 6,029,061).

Regarding claim 1, Kohlschmidt discloses a frequency adaptable semiconductor device (fig. 1), comprising:

a clock measurement and processing circuitry (103);

a radio frequency circuitry (106), communicatively coupled to the clock measurement and processing circuitry (103) that operates using first clock signal (first high accuracy clock signal from 101), and

a baseband processing circuitry (DSP 104), communicatively coupled to the clock measurement and processing circuitry (103; col 4, lines 31-34), that operates using a second clock signal (slow clock signal from 102); and

wherein the clock measurement and processing circuitry (105) is operable to receive a clock signal (received clock signals from 101 and from 102);

the clock measurement and processing circuitry determines whether the frequency of the received clock signal substantially comprises at least one of a frequency of the first clock signal and a frequency of the second clock signal (received clock signal is frequency of high accuracy clock 101 or frequency of slow clock 102; col 3, lines 10-12); and

the clock measurement and processing circuitry is operable to transform the frequency of the received clock signal substantially to at least one of the frequency of the first clock signal and the frequency of the second clock signal (the CSP calibrate the slow clock 102 to the high accuracy clock 101; col 3, lines 32-40) when the frequency of the received clock signal fails to substantially comprise at least one of the frequency of the first clock signal and the frequency of the second clock signal.

Regarding claim 5, Kohlschmidt disclose the frequency adaptable semiconductor device (fig. 1) of claim 1, wherein the clock measurement and processing circuitry further comprises a measurement circuitry;

the measurement circuitry (calibration circuitry; col 3, lines 32-40) inherently comprises a comparison circuit in order to compare the signal between the slow clock 102 and the high accuracy clock 101 to calibrate the high clock to the slow clock and a microprocessor circuitry (processor within CSP 103);

the comparison circuitry being communicatively coupled to the microprocessor circuitry within CSP 103.

Regarding claim 9, Kohlschmidt discloses the frequency adaptable semiconductor device (fig. 1) of claim 1, wherein it further comprises a low power

oscillator (low power ring oscillator at 104), communicatively coupled to the clock measurement and processing circuitry (103) (col 4, lines 52-63); and

wherein the clock measurement and processing circuitry is operable to receive the clock signal from the low power oscillator via signal line (DB/ADB) to exchange data to CSP 103 for internal clocking during low power operations.

Regarding claim 31, Kohlschmidt discloses a frequency adaptable method, comprising:

receiving a clock signal at CSP 103 input Slow CLK and High Accy CLK (fig. 1; col 3, lines 10-12);

measuring a frequency of the received clock signal (measure high clock signal from 101; col 3, lines 18-21);

determining whether the frequency of the received clock signal substantially comprises a frequency that is suitable for use as a baseband processing circuitry main system clock by a baseband processing circuitry 104 (main clock 101 during normal operation mode; col 3, lines 16-21);

determining whether the frequency of the received clock signal substantially comprises a frequency that is suitable for use as a radio frequency circuitry main system clock by a radio frequency circuitry 106 (col 4, lines 2-4);

processing the received clock signal, when the received clock signal is not suitable for use as the baseband processing circuitry main system clock, to generate a new clock signal (slow clock signal from 102) that substantially comprises a frequency that is suitable for use as the baseband processing circuitry main system clock;

and processing the received clock signal, when the received clock signal is not suitable for use as the radio frequency circuitry main system clock, to generate at least one additional new clock signal (another slow clock signal coming from 102 to output to RF section 106) that substantially comprises a frequency that is suitable for use as the radio frequency circuitry main system clock .

Regarding claim 32, Kohlschmidt discloses the method of claim 31, further comprising providing the new clock signal to the baseband processing circuitry (DSP 104 via signal bus (DB/ADB) (col 4, lines 31-34).

Regarding claim 33, Kohlschmidt discloses the method of claim 31, further comprising providing the at least one additional new clock signal to the radio frequency circuit 106 via signal line outputs to 106 (col 4, lines 2-4).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 35-36 rejected under 35 U.S.C. 103(a) as being unpatentable over Kohlschmidt (US 6,029,061).

Regarding claim 35, Kohlschmidt disclose the method of claim 31, wherein Kohlschmidt don't specifically disclose the frequency of the output signal from the external reference oscillator substantially comprises 32.768 kHz. However, the frequency from the external reference oscillator would have been chosen to output an

accurate clock signal as is well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the frequency at a specific frequency in order to output an accurate clock signal from the high accuracy clock of Kohlschmidt.

Regarding claim 36, Kohlschmidt disclose the method of claim 31, wherein Kohlschmidt does not specifically disclose the frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and the frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz. However, the frequency of the RF and DSP clock is programmed by the CSP to output the clock signal within the frequency of interest as is well known in the art. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a specific frequency based on the chosen frequency of interest for the high accuracy clock to operate correctly.

8. Claims 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohlschmidt (US 6,029,061) in view of Grundvig (US 5,844,435).

Regarding claim 46, Kohlschmidt discloses a frequency adaptable method, comprising:

starting up a semiconductor device (start normal operating mode by providing a timebase with high accuracy clock 101);

determining an operational mode of the semiconductor device (determine whether the terminal is in sleep mode or normal mode; col 3, lines 18-24).

Kohlschmidt fails to disclose:

starting up an external oscillator, the external oscillator being communicatively coupled to the semiconductor device; providing an output signal from the external oscillator to the semiconductor device; determining a frequency of the output signal from the external oscillator when the operational mode of the semiconductor device substantially comprises a low power oscillator bypass mode;

determining whether the frequency of the output signal from the external oscillator substantially comprises a frequency that is suitable for use as a main system clock by at least one circuitry portion within the semiconductor device; and

processing the output signal, from the external oscillator, to generate a new clock signal that substantially comprises a frequency that is suitable for use as the main system clock.

Grundvig discloses:

determining a frequency of the output signal from the external oscillator (12) when the operational mode of the semiconductor device substantially comprises a low power oscillator bypass mode (when not in power conserve mode, the high accuracy oscillator 12 is measured (col 2, lines 61-64);

starting up an external oscillator (12 coupled to external clock 10) to clock a first timer circuit 16, the external oscillator being communicatively coupled to the semiconductor device 18 (col 3, lines 29-37);

providing an output signal from the external oscillator 12 to the semiconductor device via 16;

determining whether the frequency of the output signal from the external oscillator 12 substantially comprises a frequency that is suitable for use as a main system clock (high accuracy clock signal) by at least one circuitry portion within the semiconductor device 18 (determining by measuring frequency variations of the high accuracy clock and the low power oscillator by processor 18); and

processing the output signal, from the external oscillator 12, to generate a new clock signal that substantially comprises a frequency that is suitable for use as the main system clock (the high accuracy clock signal is used as the processor clock source during normal operations; col 5, lines 30-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an external oscillator coupled to the high accuracy clock of Kohlschmidt in order to vary the frequency of the clock signal to output a more accurate clock signal during normal operating mode.

Regarding claim 47, Kohlschmidt and Grundvig disclose the method of claim 46, wherein Kohlschmidt discloses the at least one circuitry portion within the semiconductor device comprises at least one of a baseband processing circuitry 104 and a radio frequency circuitry 106.

Regarding claim 48, Kohlschmidt and Grundvig disclose the method of claim 47, wherein Kohlschmidt and Grundvig do not specifically disclose the frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and the frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz. However, the frequency of the RF and DSP clock is programmed

by the CSP to output the clock signal within the frequency of interest as is well known in the art. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a specific frequency based on the chosen frequency of interest for the high accuracy clock to operate correctly.

Regarding claim 49, Kohlschmidt and Grundvig disclose the method of claim 46, wherein they don't specifically disclose the frequency of the output signal from the external reference oscillator substantially comprises 32.768 kHz. However, the frequency from the external reference oscillator would have been chosen to output an accurate clock signal as is well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the frequency at a specific frequency in order to output an accurate clock signal from the high accuracy clock of Kohlschmidt.

Allowable Subject Matter

9. Claims 2-4, 6-8, 10, 34, 37-40, 50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 11-20, 21-30, 41-45, and 51-55 are allowable over the cited prior art.

11. The following is an examiner's statement of reasons for allowance:

Regarding claim 11, Kohlschmidt disclose a semiconductor device, comprising:

a baseband processing circuitry (DSP 104) that is operable to characterize a frequency of a received clock signal (received clock signal from 103; col 4, lines 45-51);

wherein the baseband processing circuitry (104) initially employs the received clock signal as a baseband processing circuitry main system clock (high accuracy clock signal in normal mode operation).

However, Kohlschmidt and the cited prior art fail to further disclose:

the baseband processing circuitry initially employs the main system clock signal when determining the feedback programming value;

a fractional-N synthesizer that is operable to generate an output clock signal having one frequency selected from among a plurality of frequencies, the selected frequency being within the fractional-N synthesizer selected using a feedback programming value;

the baseband processing circuitry feeds back the feedback programming value to the fractional-N synthesizer; and

the baseband processing circuitry subsequently operates using the output clock signal, from the fractional-N synthesizer, as the baseband processing circuitry main system clock.

Regarding claim 21, Kohlschmidt disclose a semiconductor device, comprising:

a baseband processing circuitry (CSP 103, DSP 104; fig. 1);

wherein the baseband processing circuitry (DSP 104) further comprises measurement circuitry (103) and an inherent state machine within DSP 104, the measurement circuitry (103) and the state machine (within 104) being communicatively coupled (col 4, lines 31-34);

the measurement circuitry (103) further comprises an inherent comparison circuitry and a microprocessor circuitry (processor within CSP 103), the comparison circuitry and the microprocessor circuitry being communicatively coupled, the measurement circuitry is operable to characterize a frequency of a received clock signal (received clock signal from 101 or 102);

Meador et al (US 6,747,987) disclose a fractional-N synthesizer communicatively coupled to the baseband processing circuitry; the fractional-N synthesizer further comprises a phase locked loop (PLL), a divider (205), the phase locked loop being communicatively coupled to the divider via phase detector 201 (see fig. 2).

Shepherd et al (US 5,021,754) disclose a fractional-N synthesizer 10 further comprising a multiplexor 23 (fig. 2); the divider 16 being communicatively coupled to the multiplexor via 17.

However, Kohlschmidt, Meador et al, Shepherd et al, and the cited prior art fail to further disclose:

the fractional-N synthesizer is operable to generate an output clock signal having one frequency selected from among a plurality of frequencies,

the selected frequency being within the fractional-N synthesizer selected using a feedback programming value; and

the multiplexor being communicatively coupled to a gate of the fractional N synthesizer; the baseband processing circuitry initially employs the received clock signal as a baseband processing circuitry main system clock when determining the feedback programming value; at least one of the microprocessor circuitry and the state machine

determines the feedback programming value and the baseband processing circuitry feeds back the feedback programming value to at least one of the phase locked loop, the multiplexor, and the gate of the fractional-N synthesizer; and

the baseband processing circuitry subsequently operates using the output clock signal, from the fractional-N synthesizer, as the baseband processing circuitry main system clock.

Regarding claim 51, Grundvig discloses a frequency adaptable method employed within a semiconductor device, comprising:

receiving a clock signal from an external crystal oscillator (12; col 3, lines 29-50), during power-up, determining whether at least one circuitry portion within the semiconductor device 100 employs an application that requires determination of a frequency of the received clock signal (col 2, lines 61-64);

initially employing the clock signal (high accuracy clock signal) as a main system clock (processor clock source) within the semiconductor device (col 3, lines 29-50). Kohlschmidt, Grundvig and the cited prior art fail to further disclose:

determining whether a fractional-N synthesizer, contained within the semiconductor device, initially provides the main system clock;

measuring the clock signal that is received from the external crystal oscillator; allowing a phase locked loop, contained within the fractional-N synthesizer, to lock at a system operating frequency.

resetting a microprocessor circuitry, contained within the semiconductor device;

gating off the clock signal that is received from the external crystal oscillator; programming the fractional-N synthesizer to generate a new clock signal to be used as the system clock, the system clock having the system operating frequency; and switching in the new clock signal in place of the gated off clock signal, the new clock signal thereafter being used as the system clock.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

12. Claims 41-45 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Regarding claim 41, Kohlschmidt discloses a frequency adaptable method, comprising:

determining whether an operational mode of a semiconductor device comprises a low power oscillator bypass mode (operation mode is normal);

the semiconductor device comprising a baseband processing circuitry (DSP 104), and a radio frequency circuitry (RF section 106);

Kohlschmidt fails to further disclose:

generating a clock signal using a low power oscillator when the operational mode substantially comprises the low power oscillator bypass mode.

the semiconductor device comprising the low power oscillator; receiving a clock signal from an external source when the operational fails to substantially comprise the low power oscillator bypass mode;

measuring a frequency of at least one of the generated clock signal and the received clock signal;

determining whether the frequency of at least one of the generated clock signal and the received clock signal substantially comprises a frequency that is suitable for use as a baseband processing circuitry main system clock by the baseband processing circuitry;

determining whether the frequency of at least one of the generated clock signal and the received clock signal substantially comprises a frequency that is suitable for use as a radio frequency circuitry main system clock by the radio frequency circuitry;

processing at least one of the generated clock signal and the received clock signal, when at least one of the generated clock signals and the received clock signal is not suitable for use as the baseband processing circuitry main system clock, to generate a new clock signal that substantially comprises a frequency that is suitable for use as the baseband processing circuitry main system clock; and

processing at least one of the generated clock signals and the received clock signal, when at least one of the generated clock signals and the received clock signal is not suitable for use as the radio frequency circuitry main system clock, to generate at least one additional new clock signal that substantially comprises a frequency that is suitable for use as the radio frequency circuitry main system clock.

Grundvig discloses:

generating a clock signal using a low power oscillator (24) when the operational mode substantially comprises the low power oscillator mode (power conserve mode).

the semiconductor device comprising the low power oscillator 24; receiving a clock signal from an external source (10, 12) when the operational fails to substantially comprise the low power oscillator bypass mode (in normal operations; col 5, lines 30-51);

measuring a frequency of at least one of the generated clock signal and the received clock signal (col 2, lines 61-64).

Kohlschmidt, Grundvig and the cited prior art fail to further disclose:

determining whether the frequency of at least one of the generated clock signal and the received clock signal substantially comprises a frequency that is suitable for use as a baseband processing circuitry main system clock by the baseband processing circuitry;

determining whether the frequency of at least one of the generated clock signal and the received clock signal substantially comprises a frequency that is suitable for use as a radio frequency circuitry main system clock by the radio frequency circuitry;

processing at least one of the generated clock signal and the received clock signal, when at least one of the generated clock signals and the received clock signal is not suitable for use as the baseband processing circuitry main system clock, to generate a new clock signal that substantially comprises a frequency that is suitable for use as the baseband processing circuitry main system clock; and

processing at least one of the generated clock signals and the received clock signal, when at least one of the generated clock signals and the received clock signal is not suitable for use as the radio frequency circuitry main system clock, to generate at least one additional new clock signal that substantially comprises a frequency that is suitable for use as the radio frequency circuitry main system clock.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N Le whose telephone number is (703) 308-5836. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lana Le

December 11, 2004